Lab 8

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Prelab:

A close-up of a document

Description automatically generated with low confidence

Purpose:

The purpose of lab 8 was to design a 4-bit down counter that would use a seven-segment display to display the output.

Lab Procedure:

We started the lab by opening Vivado and creating an RTL project that was set to ‘VHDL’ target language. We continued by creating a design source file called DownCounter and then copied code over from the given design file. We then modified the entity and architecture names to DownCounter.

Next, we created a simulation file titled DownCounterSim and copied code from the given simulation file and then changed the entity and architecture names to DownCounterSim. We also changed the component name to DownCounter. We then duplicated the files and modified them for an up counter.

We then ran the Behavioral Simulation and took note of the waveform output, created one final program called DownCounterTest and copied over code from the given test file. Finally, we ran Synthesis, Implementation, Generated Bitstream, and then connected the Basys 3 board to the computer and manually tested the outputs on it.

Vivado Code-

Down Counter:

Graphical user interface, text, application, email

Description automatically generatedGraphical user interface, text, application, email

Description automatically generated

Up Counter:

Graphical user interface, text, application, email

Description automatically generatedGraphical user interface, text, application

Description automatically generated

Bitstream-

Graphical user interface

Description automatically generated

Conclusion:

In this lab, we made a 4-bit down counter in Vivado that used a seven-segment display to display the outputs. The results of this lab showed the correct sequence as the counter decreased from FFFF to 0000.

Finally, I believe physically constructing a circuit is more beneficial to my learning.

Observations:

The main observation I have to improve my performance on future experiments is to learn the code more.